REMARKS

In response to the above-identified Office Action, Applicant amends the application and seek reconsideration thereof. In this reply, Applicant amends claims 1, 3, 8-10, 12-13, 16, 19, 22, 25-29, 31, 33-34, 36, 39, and 41-42, and cancel claims 2, 35, and 40. Applicant submits no new matter is added by these amendments. Applicant does not add any new claims. Accordingly, claims 1, 3-34, 36-39, and 41-42 (38 total claims, 8 independent claims) are pending.

I. Claims Rejected under 35 U.S.C. § 102

The Examiner rejects claims 1-42 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,715,096 issued to Kuge ("*Kuge*"). Applicant amends independent claims 1, 8, 13, 19, 25, 31, 34, and 39.

To anticipate a claim, the relied upon reference must disclose every element of the rejected claim. Among other elements, claims 1, 8, 13, 19, 25, 31, 34, and 39, as amended, include the elements of a sample being taken "at one of shortly after a nominal leading edge and shortly before a nominal trailing edge" of a signal. Applicant submits *Kuge* fails to teach at least these elements of claims 1, 8, 13, 19, 25, 31, 34, and 39.

In making the rejection, the Examiner characterizes *Kuge* as showing a memory controller, a delay circuit, a plurality of latches, and a comparing/analyzing circuit. In particular, the Examiner asserts that *Kuge* teaches identifying a leading edge, a trailing edge, and midpoint of a data valid window (DVW) of a timing signal.

Applicant submits, however, that *Kuge* teaches "a bus interface circuit for rapidly taking in data in synchronization with a clock signal (*Kuge*, Col. 1, lines 10-14). Furthermore, Fig. 15 in *Kuge* shows that "result register circuit 24 stores the position of the leading edge of the final effective data window detection signal relative to a

corresponding edge (rising or falling edge) of clock signal CLK" (Col. 17, lines 5-9). In addition, *Kuge* further states:

> More specifically, the position where a transition of data from "0" to "1" occurs in result register circuit 24 is the leading edge of the effective data window. The position where a transition of data from "1" to "0" occurs in result register circuit 24 is the position of the trailing edge of the clock signal corresponding to this effective data window. (Col. 17, lines 9-15).
>
> When the effective data window is substantially equal to half the cycle of clock signal CLK (when the data transfer is performed in the DDR mode), the region where "1" successively appears corresponds to the period for which the definite data bits are transferred. The central position of the latch stages storing the value of "1" in result register circuit 24 is detected and stored in strobe timing storage circuit 5c. If the effective data region is substantially equal to half the cycle of clock signal CLK, the margins for the set-up time and hold time can be maximized by obtaining the above central region (because the set-up time is made equal to the hold time). A data trigger select signal TRSEL is generated from the register at the bit position stored in strobe timing storage circuit 5c. Corresponding select circuit 6a shown in FIG. 10 is turned on, and the delayed clock signal corresponding to the register position stored in strobe timing storage circuit 5c is selected to produce strobe clock signal CKST. Therefore, the edge of strobe clock signal CKST changes substantially at the central region of the effective data, and the corresponding effective data is sampled. (Col. 17, lines 16-35).

As such, Applicant submits *Kuge* teaches a system where a sample is taken only at the rising and falling edges of the signal. Therefore, *Kuge* fails to teach at least a sample taken at one of shortly after a nominal leading edge and shortly before a trailing edge.

The failure of *Kuge* to teach each of the elements of claims 1, 8, 13, 19, 25, 31, 34, and 39 is fatal to the anticipation rejection. Therefore, claims 1, 8, 13, 19, 25, 31, 34,

and 39 are not anticipated by *Kuge*. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1, 8, 13, 19, 25, 31, 34, and 39.

Claims 3-7, 9-12, 14-18, 20-24, 26-30, 32-33, 36-38, and 41-42 each either directly or indirectly depends from independent claims 1, 8, 13, 19, 25, 31, 34, and 39. Therefore, Applicant submits claims 3-7, 9-12, 14-18, 20-24, 26-30, 32-33, 36-38, and 41-42 are not anticipated by *Kuge* at least for the same reasons as independent claims 1, 8, 13, 19, 25, 31, 34, and 39, in addition to their own respective features. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 3-7, 9-12, 14-18, 20-24, 26-30, 32-33, 36-38, and 41-42.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending are in condition for allowance. A Notice of Allowance if earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned.

If necessary, the Commissioner is hereby authorized to charge payment or credit any overpayment to Deposit Account No. 1928-14 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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